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EXAMINER
JOHNSON, CARLTON

ART UNIT	PAPER NUMBER
2136	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,125	PAI ET AL.	
	Examiner	Art Unit	
	Carlton V. Johnson	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to application papers filed on **8-13-2003**.

2. Claims **1 - 17** are pending. Claims **1, 9, 17** are independent.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim **1 - 3, 5 - 11, 13 - 16** are rejected under 35 U.S.C. 102(e) as being anticipated by **Katsavounidis et al.** (US PGPUB No. **20020181594**).

Regarding Claim 1, Katsavounidis discloses a method for providing a plurality of sequential data words, said method comprising:

a) receiving a command to provide the plurality of sequential data words, wherein the plurality of sequential data words comprises a first data word and a last data word, and one or more data words between the first data word and the last data word; (see Katsavounidis paragraph [0040], lines 1-4; paragraph [0041], lines 14-

18: input (command) to decode data; paragraph [0176], lines 6-11; paragraph [0120], lines 5-8; paragraph [0121], lines 4-8; paragraph [0173], line 4: process sequential data words; multiple words (first, last))

b) fetching a sequential portion of the sequential data words, said sequential portion comprising a first intermediate word, the last word, and one or more data words between the intermediate word and the last word; (see Katsavounidis paragraph [0120], lines 5-8: buffer portion for processing)

c) storing the sequential portion; (see Katsavounidis paragraph [0183], lines 3-8; paragraph [0131], lines 5-8: buffer storage)

d) transmitting at least a portion of the last data word in reverse bit position order; (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit order based on sign bit) and

d) transmitting at least a portion of the intermediate data words after transmitting at least the portion of the last data word in reverse bit position order. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse word order)

Regarding Claim 2, Katsavounidis discloses the method of claim 1, further comprising:

a) fetching another sequential portion of the sequential data words, the another sequential portion comprising a second intermediate data word, immediately followed by one or more data words, immediately followed by a third intermediate data word, the third intermediate data word immediately preceding the first

intermediate word; (see Katsavounidis paragraph [0125], lines 6-9: process another block of data)

b) storing the another sequential portion; (see Katsavounidis paragraph [0183], lines 3-8; paragraph [0131], lines 5-8: buffer storage)

c) transmitting at least a portion of the third intermediate word in reverse bit position order; (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit order based on sign bit) and

d) transmitting at least a portion of the second intermediate word after transmitting at least the portion of the third intermediate word in reverse bit position order. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit, word order)

Regarding Claims 3, 11, Katsavounidis discloses the method, system of claims 1, 9, wherein storing further comprises: storing the sequential portion in a memory, the memory having a beginning address and an ending address, and wherein at least the portion of the last data word is stored at the ending address and wherein at least the portion of the first intermediate word is stored in the beginning address. (see Katsavounidis paragraph [0042], lines 3-12; paragraph [0015], lines 8-16: addressable memory storage for data, forward processing direction, first word, last word)

Regarding Claims 5, 13, Katsavounidis discloses the method, system of claims 3, 11, wherein the last data word comprises at least the portion of the last data word and at

least another portion, wherein at least the portion comprises the least significant bits of the last data word, and wherein the at least another portion comprises the most significant bits of the last data word, and wherein storing the portion further comprises: storing the at least another portion of the last data word at an address preceding the ending address. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit order, based on sign bit, process data in reverse word order, last word is first word)

Regarding Claim 6, Katsavounidis discloses the method of claim 5, further comprising: transmitting the at least another portion of the last word in reverse bit position order after transmitting at least the portion of the last word in reverse bit position order. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit level order, based on sign bit)

Regarding Claims 7, 15, Katsavounidis discloses the method, system of claims 1, 9, wherein the one or more data words comprise a predetermined number of data words. (see Katsavounidis paragraph [0173], line 4: number of data words to process)

Regarding Claims 8, 16, Katsavounidis discloses the method, system of claims 1, 9, wherein the plurality of sequential data words stores a slice group. (see Katsavounidis paragraph [0120], lines 5-8: block, processing group of sequential words (slice group))

Regarding Claim 9, Katsavounidis discloses a system for providing a plurality of sequential data words, said method comprising:

a) a state logic machine for receiving a command to provide the plurality of sequential of sequential data words, the plurality of sequential data words comprises a first data word and a last data word, and one or more data words between the first data word and the last data word; (see Katsavounidis paragraph [0176], lines 6-11; paragraph [0120], lines 5-8; paragraph [0121], lines 4-8; paragraph [0173], line 4: process sequential data words, multiple words (first, last))

b) a memory controller for fetching a sequential portion of the sequential data words, said sequential portion comprising a first intermediate word, the last word, and one or more data words between the intermediate word and the last word; (see Katsavounidis paragraph [0042], lines 3-12: addressable memory storage for data; paragraph [0015], lines 8-16: forward processing direction, first word, last word)

c) a local buffer for storing the sequential portion; (see Katsavounidis paragraph [0183], lines 3-8; paragraph [0131], lines 5-8: buffer storage) and

d) a plurality of multiplexers for reversing bit positions of at least a portion of the last data word and reversing bit positions of at least a portion of the intermediate data word; (see Katsavounidis paragraph [0135], lines 1-5: reverse bit processing, reverse buffer (word) processing)

e) a port for transmitting at least a portion of the last data word in the reverse bit position order and transmitting at least a portion of the intermediate data word in reverse bit position order after transmitting at least the portion of the last data word. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit order, based on sign bit, process data in reverse word order, last word is first word)

Regarding Claim 10, Katsavounidis discloses the system of claim 9, wherein:

a) the memory controller fetches another sequential portion of the sequential data words, the another sequential portion comprising a second intermediate data word, immediately followed by one or more data words, immediately followed by a third intermediate data word, the third intermediate data word immediately preceding the first intermediate word; (see Katsavounidis paragraph [0125], lines 6-9: process another block of data))

b) the local buffer stores the another sequential portion; (see Katsavounidis paragraph [0183], lines 3-8; paragraph [0131], lines 5-8: buffer storage) and

c) the port transmits at least a portion of the third intermediate word and transmits at least a portion of the second intermediate word after transmitting at least the portion of the third intermediate word. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data in reverse bit order based on sign bit, reverse word order, third and then second word processed)

Regarding Claim 14, Katsavounidis discloses the system of claim 13, wherein the port transmits the at least another portion of the last word after transmitting at least the portion of the last word. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 5-11: process data at bit level order, based on sign bit)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **4, 12, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Katsavounidis** in view of **Ouyang et al.** (US Patent No. **7,085,320**).

Regarding Claims 4, 12, Katsavounidis discloses the method of claims 3, 11. Ouyang discloses wherein the memory is characterized by a width, and the data words are characterized by a width, the width of the memory being smaller than the width of the data words. (see Ouyang col. 12, lines 35-40: memory width less than word width, multiple reads)

It would have been obvious to one of ordinary skill in the art to modify Katsavounidis as taught by Ouyang to enable the capability to enable the usage of a direct memory access engine. One of ordinary skill in the art would have been

motivated to employ the teachings of Tojima in order to enable the capability to enable the flexibility for the easy implementation of video compression based on all state-of-the-art standards. (see Ouyang col. 2, lines 36-40: " ... *Accordingly, what is needed is a versatile video compression scheme that enables the dynamic selection of video output formats. The scheme should have sufficient flexibility to allow for the easy implementation of video compression based on all state-of-the-art standards.* ... ")

Regarding Claim 17, Katsavounidis discloses a system for decoding a slice group, said system comprising:

a) a compressed data buffer comprising a plurality of sequential data words, the plurality of sequential data words for storing a slice group; (see Katsavounidis paragraph [0186], lines 10-12: compression utilized in storage buffer)

b) a video decoder for decoding the slice group; (see Katsavounidis paragraph [0014], lines 7-14; paragraph [0042], lines 1-3: decoder, decoding buffer of sequential group of words (slice)) and

the memory access engine comprising:

d) a state logic machine for receiving a command to provide the plurality of sequential data words and a control signal indicating reverse order from the video decoder, the plurality of sequential data words comprises a first data word and a last data word, and one or more data words between the first data word and the last data word; (see Katsavounidis paragraph [0133], lines 7-13;

paragraph [0135], lines 5-11: process data in reverse bit order, based on sign bit, process data in reverse word order, last word is first word)

e) a memory controller for fetching a sequential portion of the sequential data words, said sequential portion comprising a first intermediate word, the last word, and one or more data words between the intermediate word and the last word; (see Katsavounidis paragraph [0042], lines 3-12: memory controller)

f) a local buffer for storing the sequential portion; (see Katsavounidis paragraph [0183], lines 3-8; paragraph [0131], lines 5-8: buffer storage)

g) a plurality of multiplexers for reversing the bit positions of the first intermediate word and the last data word; (see Katsavounidis paragraph [0135], lines 1-5: reverse bit processing, reverse buffer (word) processing) and

h) a port for transmitting at least a portion of the last data word in reverse bit position order and transmitting at least a portion of the intermediate data words in reverse bit position order after transmitting at least the portion of the last data word. (see Katsavounidis paragraph [0133], lines 7-13; paragraph [0135], lines 3-11: reverse bit processing of codeword(s), data)

Katsavounidis does not specifically disclose a direct memory access engine.

However, Ouyang, in the same field of endeavor, discloses:

c) a direct memory access engine for providing the slice group to the video decoder,

(see Ouyang col. 2, lines 60-61; col. 13, line 5-10: media data decoding (MPEG-4); col. 11, lines 52-62; col. 13, lines 1-3: DMA controller)

It would have been obvious to one of ordinary skill in the art to modify Katsavounidis as taught by Ouyang to enable the capability to enable the usage of a direct memory access engine. One of ordinary skill in the art would have been motivated to employ the teachings of Tojima in order to enable the capability to enable the flexibility for the easy implementation of video compression based on all state-of-the-art standards. (see Ouyang col. 2, lines 36-40)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C. J.
CVJ
May 28, 2007

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6/6/07

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